



VN800S VN800PT

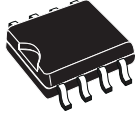
HIGH SIDE DRIVER

TYPE	$R_{DS(on)}$	I_{OUT}	V_{CC}
VN800S VN800PT	135 m Ω	0.7 A	36 V

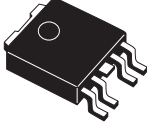
- CMOS COMPATIBLE INPUT
- THERMAL SHUTDOWN
- CURRENT LIMITATION
- SHORTED LOAD PROTECTION
- UNDERVOLTAGE AND OVERVOLTAGE SHUTDOWN
- PROTECTION AGAINST LOSS OF GROUND
- VERY LOW STAND-BY CURRENT
- REVERSE BATTERY PROTECTION (*)

DESCRIPTION

The VN800S, VN800PT are monolithic devices made by using STMicroelectronics VIPower M0-3 Technology, intended for driving any kind of load with one side connected to ground. Active V_{CC} pin voltage clamp protects the device against low energy spikes. Active current limitation combined with thermal shutdown and



SO-8

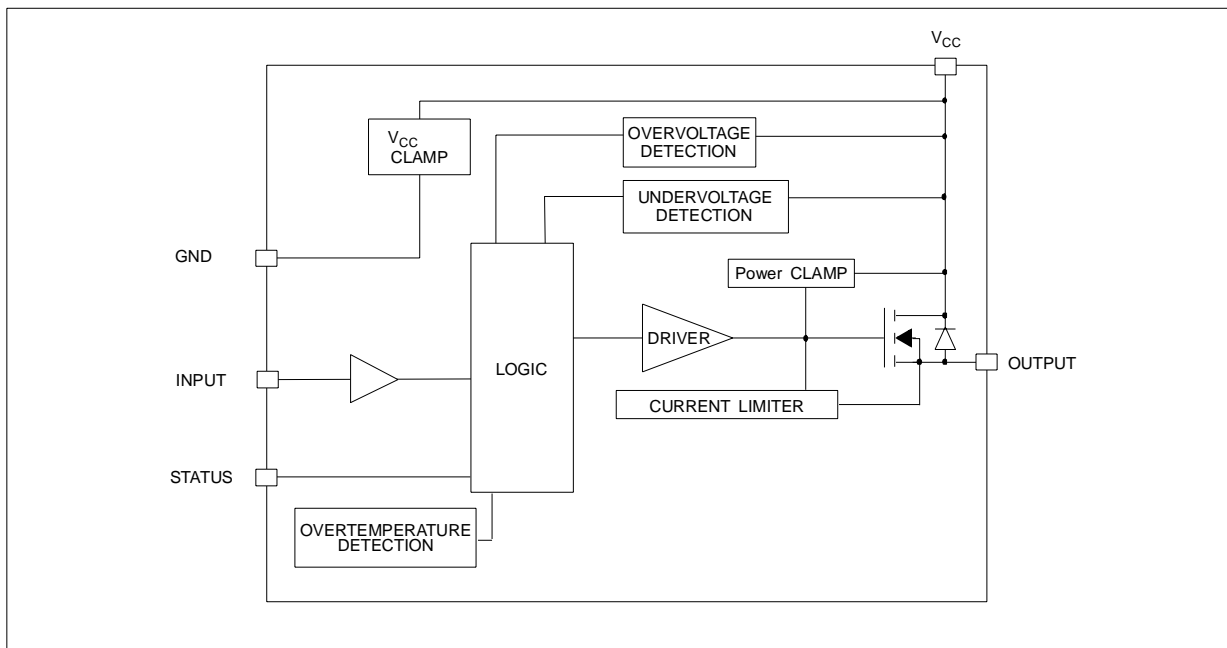


PPAK

ORDER CODES		
PACKAGE	TUBE	T&R
SO-8	VN800S	VN800S13TR
PPAK	VN800PT	VN800PT13TR

automatic restart protect the device against overload. Device automatically turns off in case of ground pin disconnection. This device is especially suitable for industrial applications in norms conformity with IEC1131 (Programmable Controllers International Standard).

BLOCK DIAGRAM

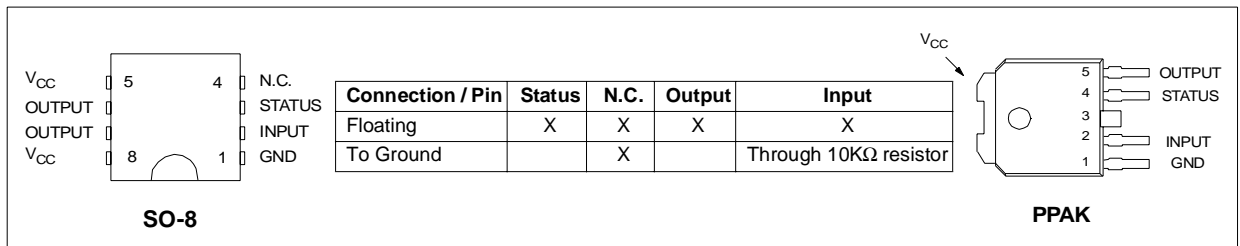


(*) See note at page 7

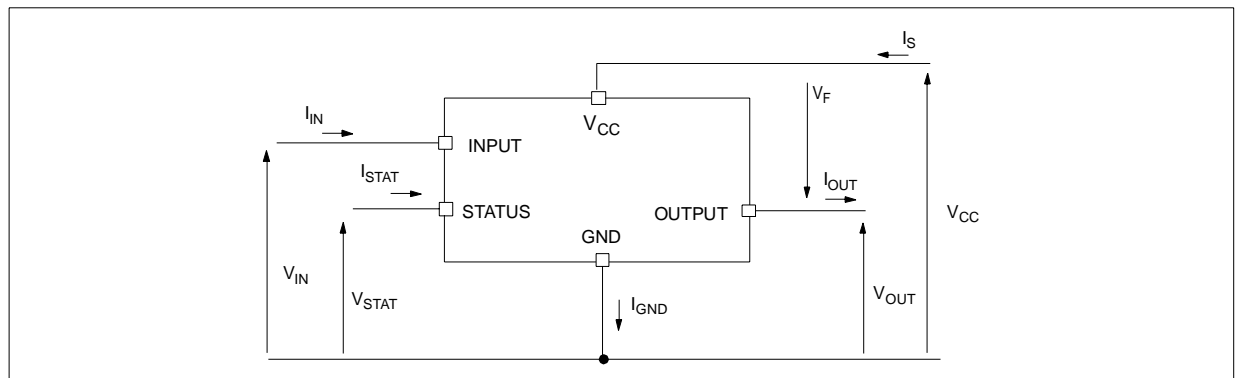
ABSOLUTE MAXIMUM RATING

Symbol	Parameter	Value		Unit
		SO-8	PPAK	
V_{CC}	DC Supply Voltage	41		V
$-V_{CC}$	Reverse DC Supply Voltage	- 0.3		V
$-I_{GND}$	DC Reverse Ground Pin Current	- 200		mA
I_{OUT}	DC Output Current	Internally Limited		A
$-I_{OUT}$	Reverse DC Output Current	- 6		A
I_{IN}	DC Input Current	+/- 10		mA
V_{IN}	Input Voltage Range	$-3/+V_{CC}$		V
V_{STAT}	DC Status Voltage	$+ V_{CC}$		V
V_{ESD}	Electrostatic Discharge (Human Body Model: $R=1.5K\Omega$; $C=100pF$)			
	- INPUT	4000		V
	- STATUS	4000		V
	- OUTPUT	5000		V
	- V_{CC}	5000		V
P_{tot}	Power Dissipation $T_C=25^\circ C$	4.2	41.7	W
E_{MAX}	Maximum Switching Energy ($L=77.5mH$; $R_L=0\Omega$; $V_{bat}=13.5V$; $T_{jstart}=150^\circ C$; $I_L=1.5A$)	121		mJ
E_{MAX}	Maximum Switching Energy ($L=125mH$; $R_L=0\Omega$; $V_{bat}=13.5V$; $T_{jstart}=150^\circ C$; $I_L=1.5A$)		195	mJ
T_j	Junction Operating Temperature	Internally Limited		$^\circ C$
T_C	Case Operating Temperature	- 40 to 150		$^\circ C$
T_{stg}	Storage Temperature	- 55 to 150		$^\circ C$
L_{max}	Max Inductive Load ($V_{CC}=30V$; $I_{LOAD}=0.5A$; $T_{amb}=100^\circ C$; $R_{thcase>ambient}\leq 25^\circ C/W$)		2	H

CONFIGURATION DIAGRAM (TOP VIEW) & SUGGESTED CONNECTIONS FOR UNUSED AND N.C. PINS



CURRENT AND VOLTAGE CONVENTIONS



THERMAL DATA

Symbol	Parameter		Value		Unit
			SO-8	PPAK	
R _{thj-case}	Thermal Resistance Junction-case	Max	-	3	°C/W
R _{thj-lead}	Thermal Resistance Junction-lead	Max	30	-	°C/W
R _{thj-amb}	Thermal Resistance Junction-ambient	Max	93 ⁽¹⁾	78 ⁽³⁾	°C/W
		Max	82 ⁽²⁾	45 ⁽⁴⁾	°C/W

⁽¹⁾ When mounted on FR4 printed circuit board with 0.5 cm² of copper area (at least 35μ thick) connected to all V_{CC} pins.

⁽²⁾ When mounted on FR4 printed circuit board with 2 cm² of copper area (at least 35μ thick).

⁽³⁾ When mounted on FR4 printed circuit board with 0.5 cm² of copper area (at least 35μ thick) connected to all V_{CC} pins.

⁽⁴⁾ When mounted on FR4 printed circuit board with 6 cm² of copper area (at least 35μ thick).

ELECTRICAL CHARACTERISTICS (8V < V_{CC} < 36V; -40°C < T_J < 150°C, unless otherwise specified)

POWER

Symbol	Parameter	Test Conditions	Min	Typ	Max	Unit
V _{CC}	Operating Supply Voltage		5.5		36	V
V _{USD}	Undervoltage Shut-down		3	4	5.5	V
V _{OV}	Overvoltage Shut-down		36	42		V
R _{ON}	On State Resistance	I _{OUT} = 0.5A; T _J = 25°C			135	mΩ
		I _{OUT} = 0.5A			270	mΩ
I _S	Supply Current	Off State; V _{CC} = 24V; T _{case} = 25°C		10	20	μA
		On State; V _{CC} = 24V		1.5	3.5	mA
		On State; V _{CC} = 24V; T _{case} = 100°C				2.6
I _{LGND}	Output Current at turn-off	V _{CC} = V _{STAT} = V _{IN} = V _{GND} = 24V; V _{OUT} = 0V			1	mA
I _{L(off1)}	Off State Output Current	V _{IN} = V _{OUT} = 0V	0		50	μA
I _{L(off2)}	Off State Output Current	V _{IN} = V _{OUT} = 0V; V _{CC} = 13V; T _J = 125°C			5	μA
I _{L(off3)}	Off State Output Current	V _{IN} = V _{OUT} = 0V; V _{CC} = 13V; T _J = 25°C			3	μA

SWITCHING (V_{CC} = 24V)

Symbol	Parameter	Test Conditions	Min	Typ	Max	Unit
t _{d(on)}	Turn-on Delay Time	R _L = 48Ω from V _{IN} rising edge to V _{OUT} = 2.4V		10		μs
t _{d(off)}	Turn-off Delay Time	R _L = 48Ω from V _{IN} falling edge to V _{OUT} = 21.6V		40		μs
dV _{OUT} /dt _(on)	Turn-on Voltage Slope	R _L = 48Ω from V _{OUT} = 2.4V to V _{OUT} = 19.2V		See relative diagram		V/μs
dV _{OUT} /dt _(off)	Turn-off Voltage Slope	R _L = 48Ω from V _{OUT} = 21.6V to V _{OUT} = 2.4V		See relative diagram		V/μs

INPUT PIN

Symbol	Parameter	Test Conditions	Min	Typ	Max	Unit
V _{INL}	Input Low Level				1.25	V
I _{INL}	Low Level Input Current	V _{IN} = 1.25V	1			μA
V _{INH}	Input High Level		3.25			V
I _{INH}	High Level Input Current	V _{IN} = 3.25V			10	μA
V _{I(hyst)}	Input Hysteresis Voltage		0.5			V
I _{IN}	Input Current	V _{IN} = V _{CC} = 36V			200	μA

VN800S / VN800PT

ELECTRICAL CHARACTERISTICS (continued)

VCC - OUTPUT DIODE

Symbol	Parameter	Test Conditions	Min	Typ	Max	Unit
V_F	Forward on Voltage	$-I_{OUT}=0.6A$; $T_j=150^\circ C$			0.7	V

STATUS PIN

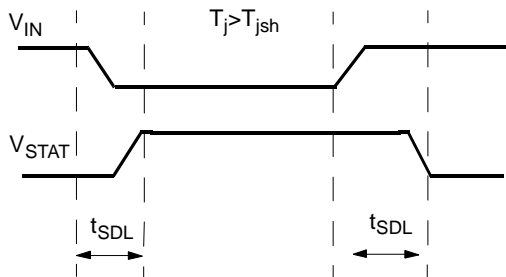
Symbol	Parameter	Test Conditions	Min	Typ	Max	Unit
V_{STAT}	Status Low Output Voltage	$I_{STAT}=1.6\text{ mA}$			0.5	V
I_{LSTAT}	Status Leakage Current	Normal Operation; $V_{STAT}=V_{CC}=36\text{ V}$			10	μA
C_{STAT}	Status Pin Input Capacitance	Normal Operation; $V_{STAT}=5\text{ V}$			30	pF

PROTECTIONS (see note 1)

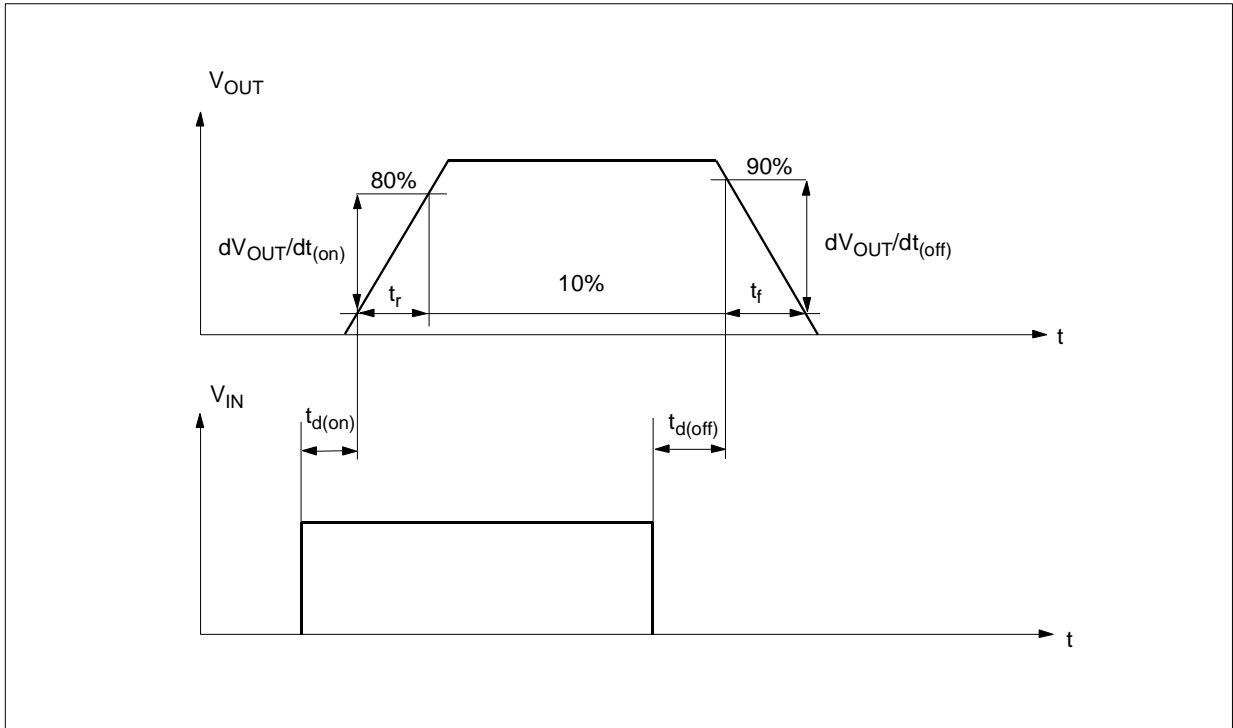
Symbol	Parameter	Test Conditions	Min	Typ	Max	Unit
T_{TSD}	Shut-down Temperature		150	175	200	$^\circ C$
T_R	Reset Temperature		135			$^\circ C$
T_{hyst}	Thermal Hysteresis		7	15		$^\circ C$
T_{SDL}	Status Delay in Overload Condition	$T_j > T_{jsh}$			20	μs
I_{lim}	DC Short Circuit Current	$V_{CC}=24\text{ V}$; $R_{LOAD}=10\text{ m}\Omega$	0.7		2	A
V_{demag}	Turn-off Output Clamp Voltage	$I_{OUT}=0.5\text{ A}$; $L=6\text{ mH}$	$V_{CC}-47$	$V_{CC}-52$	$V_{CC}-57$	V

Note 1: To ensure long term reliability under heavy overload or short circuit conditions, protection and related diagnostic signals must be used together with a proper software strategy. If the device operates under abnormal conditions this software must limit the duration and number of activation cycles.

OVERTEMP STATUS TIMING



Switching time Waveforms



TRUTH TABLE

CONDITIONS	INPUT	OUTPUT	STATUS
Normal Operation	L	L	H
	H	H	H
Current Limitation	L	L	H
	H	X	$(T_j < T_{TSD})$ H
	H	X	$(T_j > T_{TSD})$ L
Overtemperature	L	L	H
	H	L	L
Undervoltage	L	L	X
	H	L	X
Overvoltage	L	L	H
	H	L	H

Figure 1: Peak Short Circuit Current Test Circuit

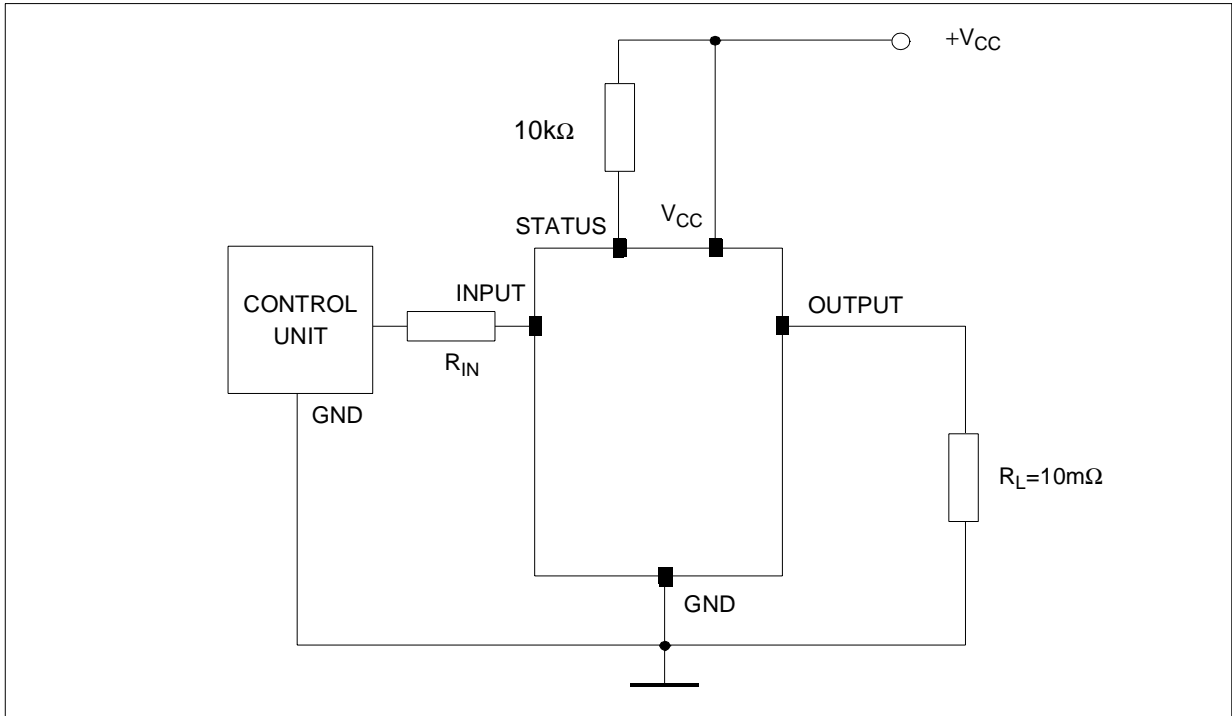
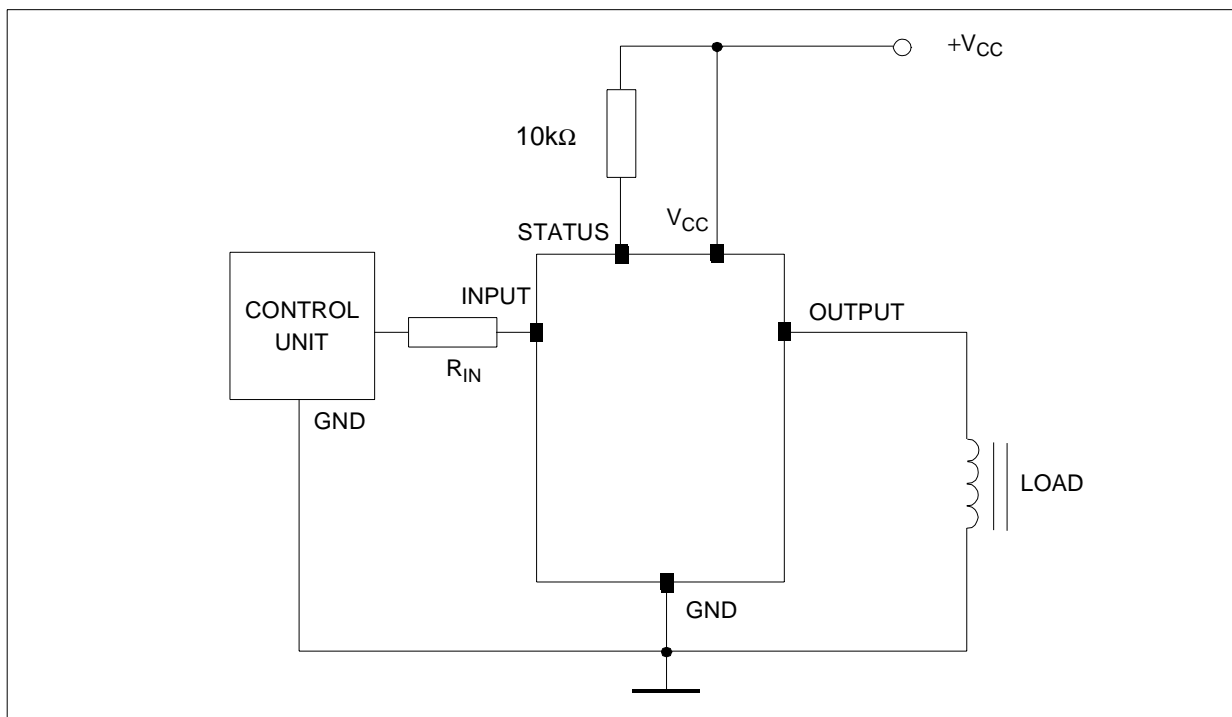
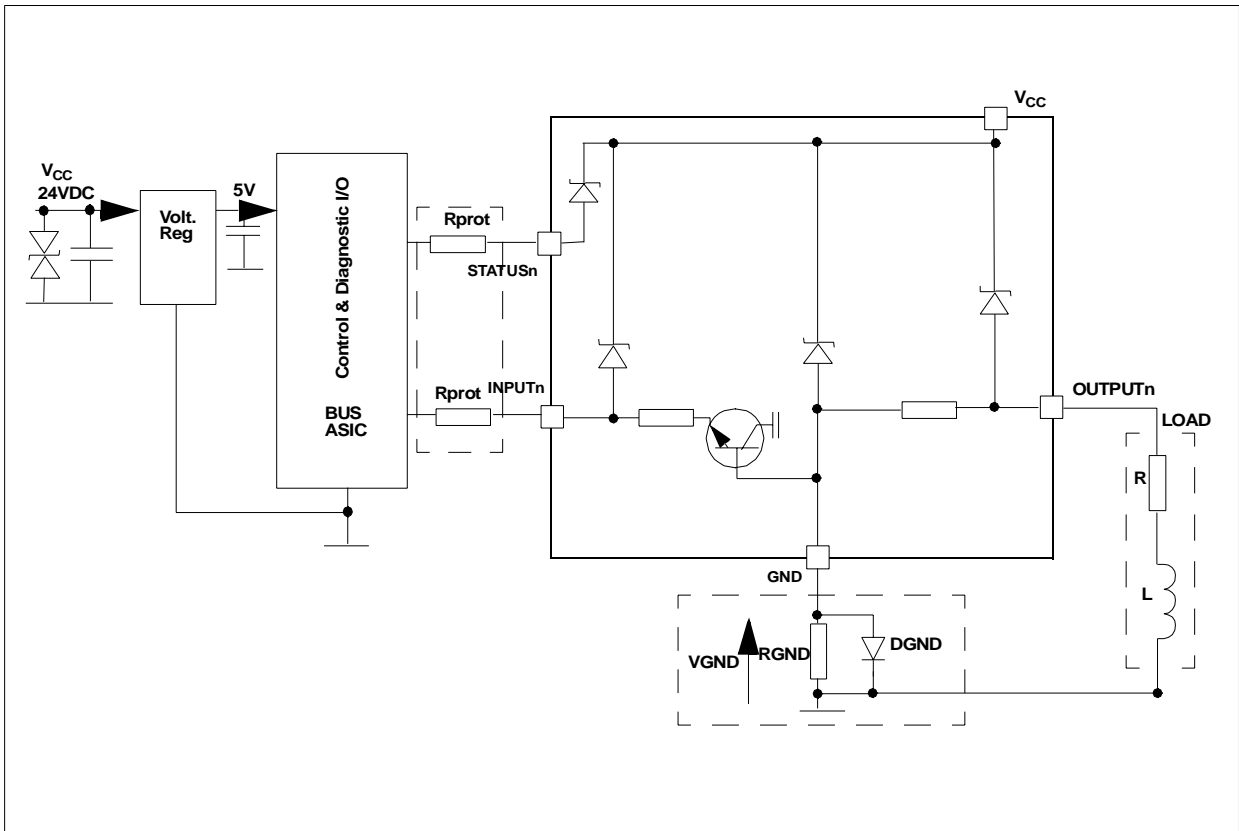


Figure 2: Avalanche Energy Test Circuit



APPLICATION SCHEMATIC



GND PROTECTION NETWORK AGAINST REVERSE BATTERY

Solution 1: Resistor in the ground line (R_{GND} only). This can be used with any type of load.

The following is an indication on how to dimension the R_{GND} resistor.

- 1) $R_{GND} \leq 600\text{mV} / (I_{S(on)max})$.
- 2) $R_{GND} \geq (-V_{CC}) / (-I_{GND})$

where $-I_{GND}$ is the DC reverse ground pin current and can be found in the absolute maximum rating section of the device's datasheet.

Power Dissipation in R_{GND} (when $V_{CC} < 0$: during reverse battery situations) is:

$$P_D = (-V_{CC})^2 / R_{GND}$$

This resistor can be shared amongst several different HSD. Please note that the value of this resistor should be calculated with formula (1) where $I_{S(on)max}$ becomes the sum of the maximum on-state currents of the different devices.

Please note that if the microprocessor ground is not common with the device ground then the R_{GND} will produce a shift ($I_{S(on)max} * R_{GND}$) in the input thresholds and the status output values. This shift will vary depending on many devices are ON in the case of several high side drivers sharing the same R_{GND} .

If the calculated power dissipation leads to a large resistor or several devices have to share the same resistor then the ST suggests to utilize Solution 2 (see below).

Solution 2: A diode (D_{GND}) in the ground line.

A resistor ($R_{GND} = 1\text{k}\Omega$) should be inserted in parallel to D_{GND} if the device will be driving an inductive load.

This small signal diode can be safely shared amongst several different HSD. Also in this case, the presence of the ground network will produce a shift ($\approx 600\text{mV}$) in the input threshold and the status output values if the microprocessor ground is not common with the device ground. This shift will not vary if more than one HSD shares the same diode/resistor network.

Series resistor in INPUT and STATUS lines are also required to prevent that, during battery voltage transient, the current exceeds the Absolute Maximum Rating.

Safest configuration for unused INPUT and STATUS pin is to leave them unconnected.

μC I/Os PROTECTION:

If a ground protection network is used and negative transients are present on the V_{CC} line, the control pins will be pulled negative. ST suggests to insert a resistor (R_{prot}) in line to prevent the μC I/Os pins to latch-up.

The value of these resistors is a compromise between the leakage current of μC and the current required by the HSD I/Os (Input levels compatibility) with the latch-up limit of μC I/Os.

$$-V_{CCpeak} / I_{latchup} \leq R_{prot} \leq (V_{OH\mu C} - V_{IH} - V_{GND}) / I_{IHmax}$$

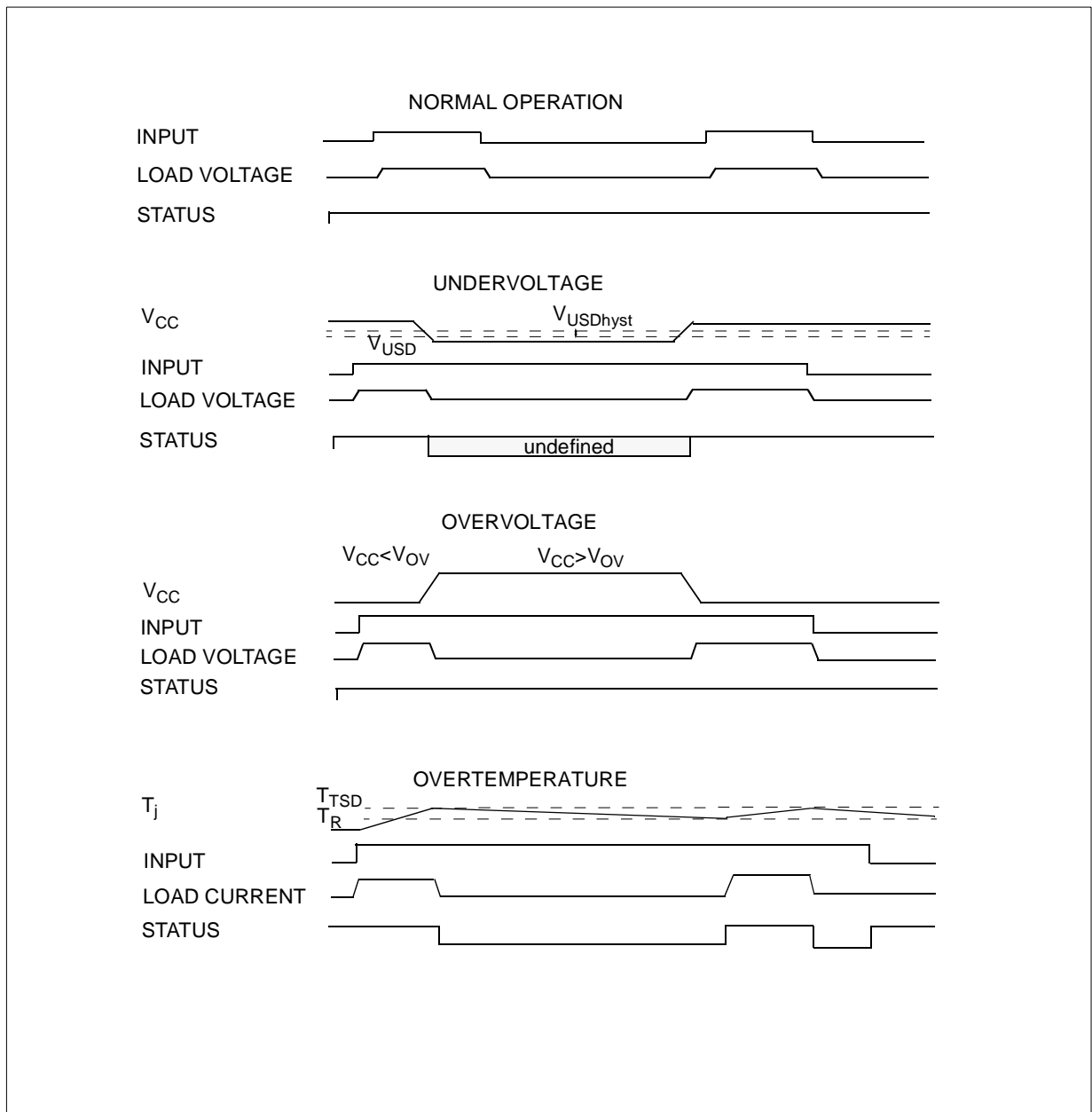
Calculation example:

For $V_{CCpeak} = -100\text{V}$ and $I_{latchup} \geq 20\text{mA}$; $V_{OH\mu C} \geq 4.5\text{V}$

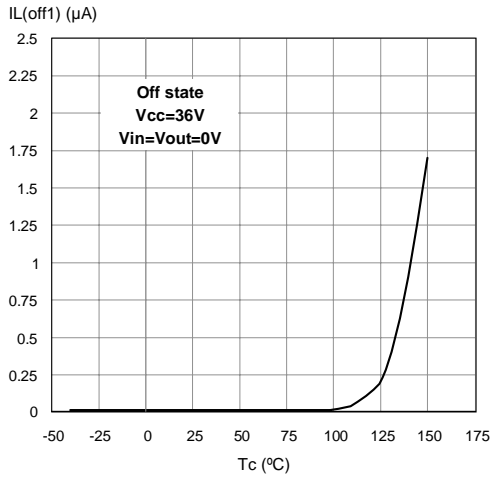
$$5\text{k}\Omega \leq R_{prot} \leq 65\text{k}\Omega$$

Recommended R_{prot} value is $10\text{k}\Omega$.

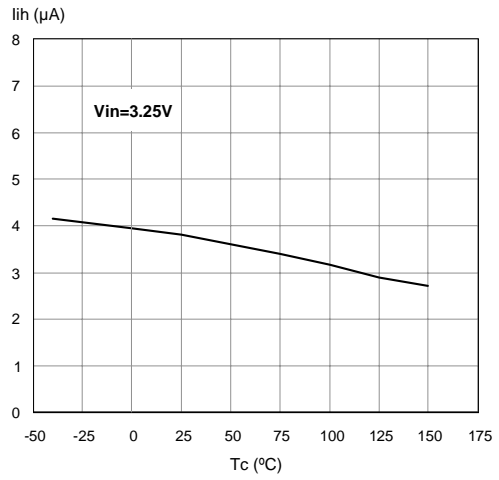
Figure 3: Waveforms



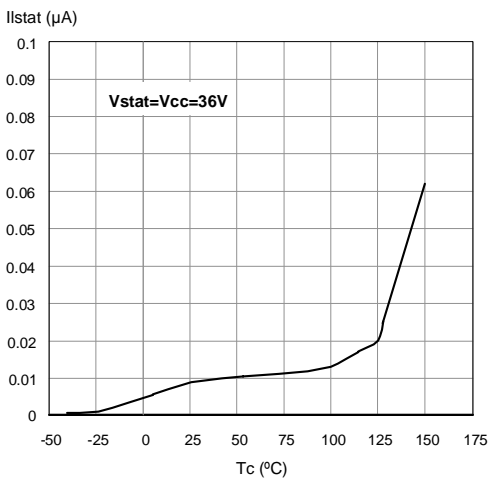
Off State Output Current



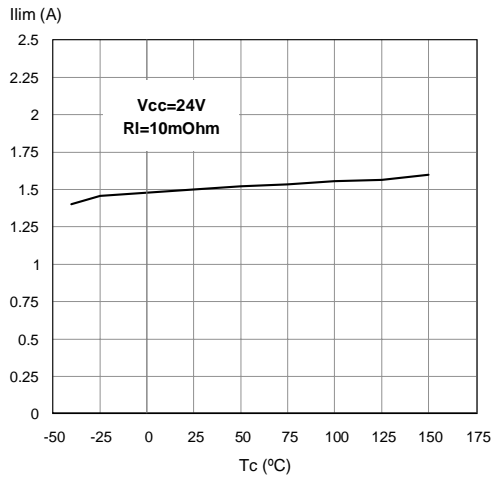
High Level Input Current



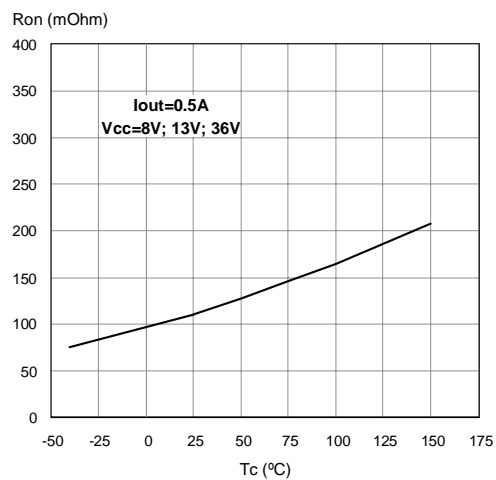
Status Leakage Current



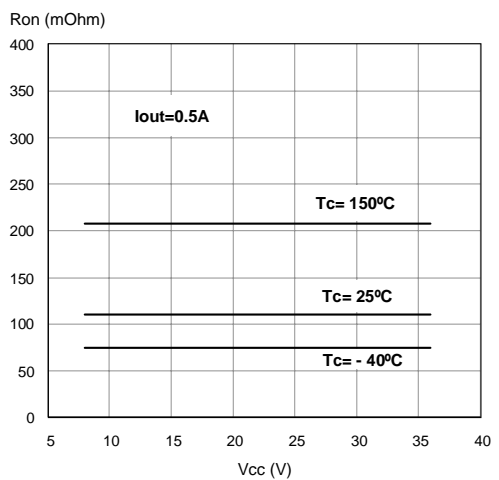
I_{LIM} Vs T_{case}



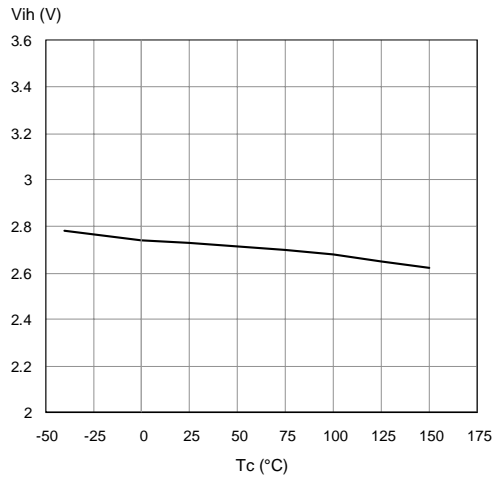
On State Resistance Vs T_{case}



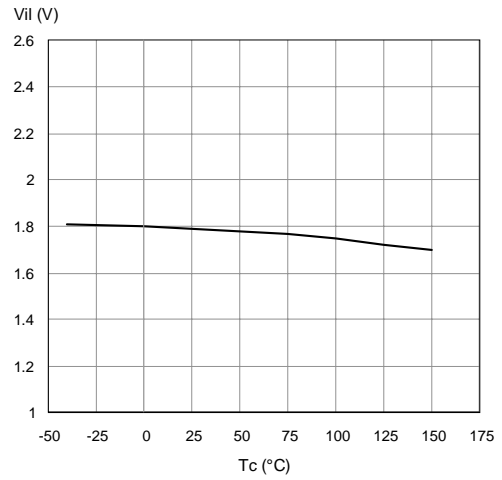
On State Resistance Vs V_{CC}



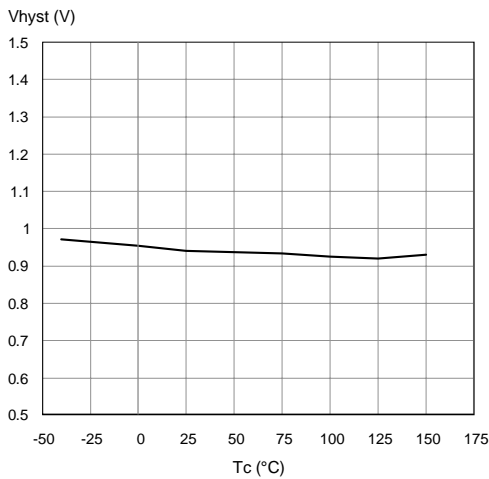
Input High Level



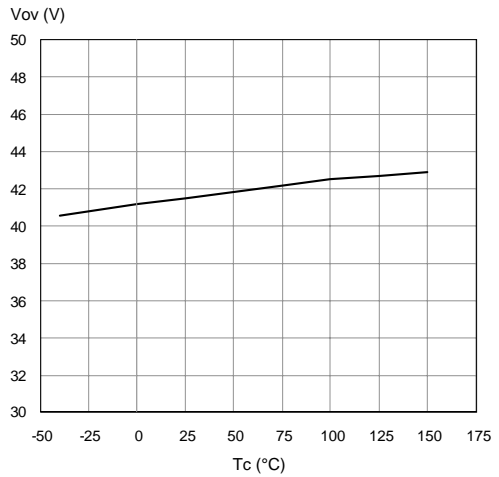
Input Low Level



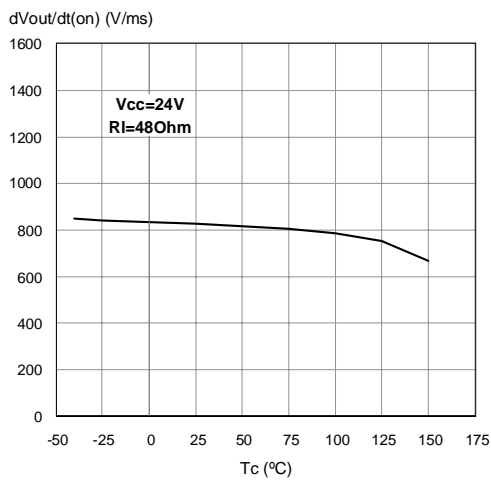
Input Hysteresis Voltage



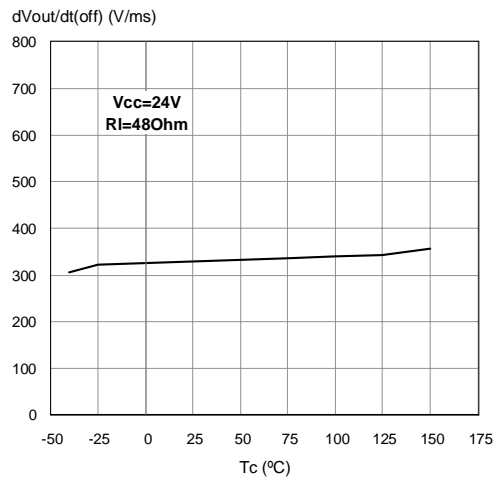
Overvoltage Shutdown



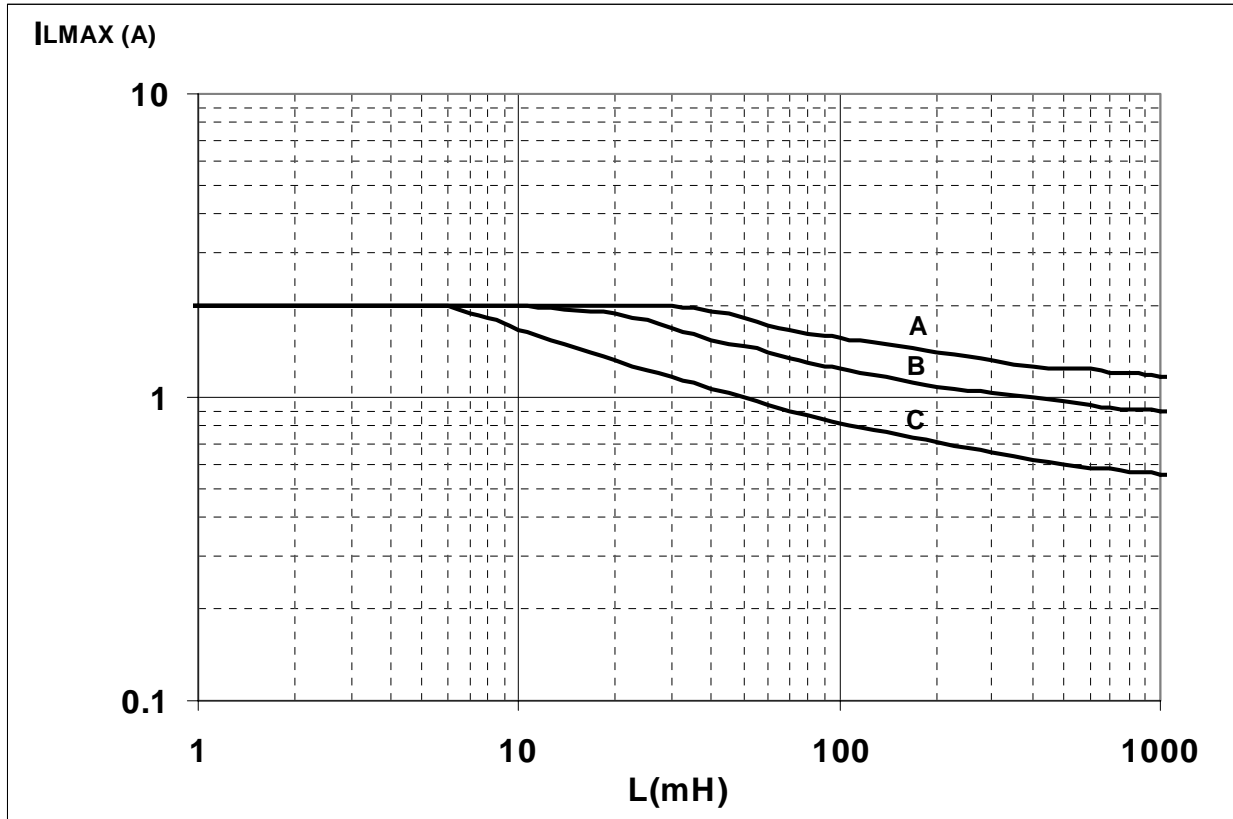
Turn-on Voltage Slope



Turn-off Voltage Slope



PPAK Maximum turn off current versus load inductance



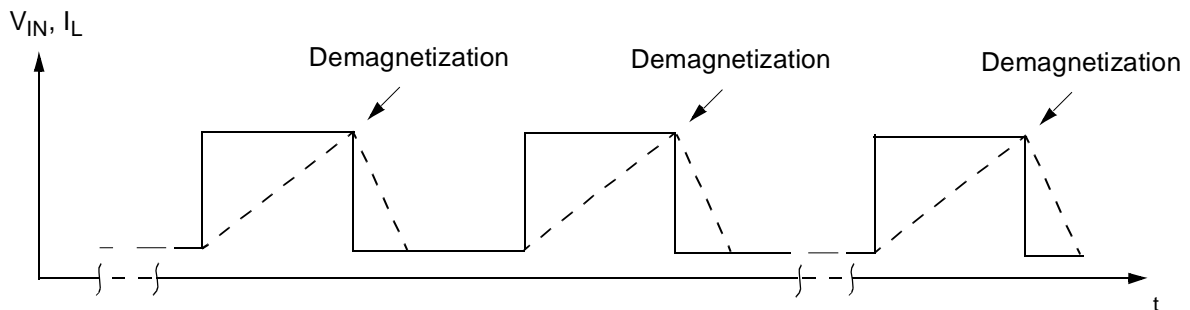
- A = Single Pulse at $T_{Jstart}=150^{\circ}C$
- B= Repetitive pulse at $T_{Jstart}=100^{\circ}C$
- C= Repetitive Pulse at $T_{Jstart}=125^{\circ}C$

Conditions:

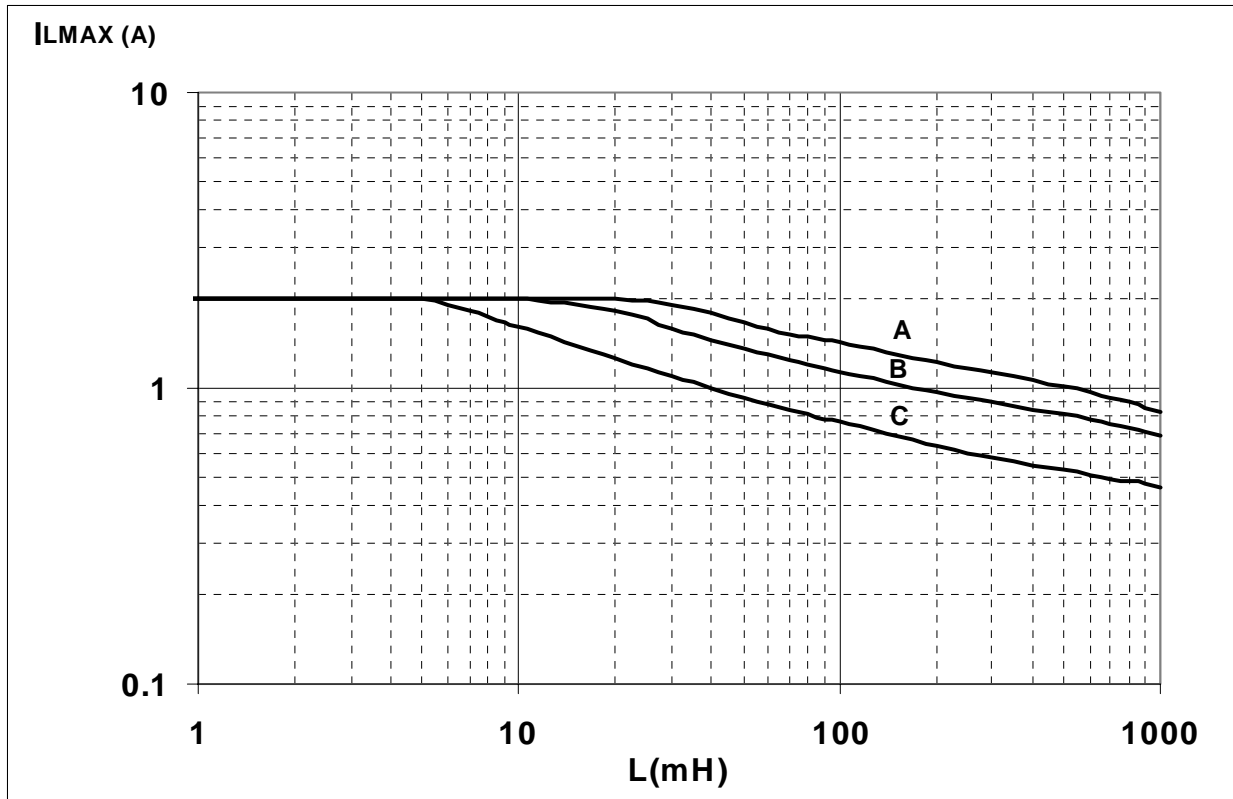
$V_{CC}=13.5V$

Values are generated with $R_L=0\Omega$

In case of repetitive pulses, T_{Jstart} (at beginning of each demagnetization) of every pulse must not exceed the temperature specified above for curves B and C.



SO-8 Maximum turn off current versus load inductance



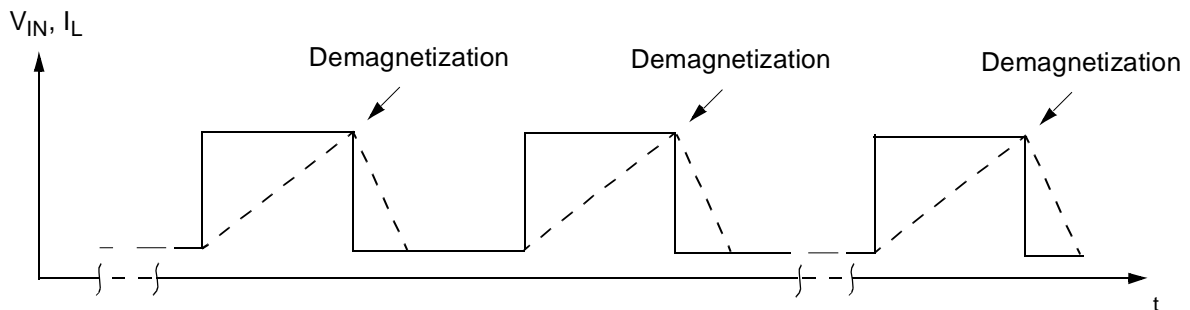
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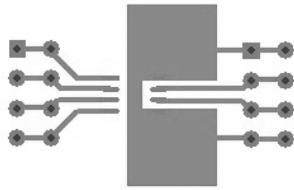


SO-8 THERMAL DATA

SO-8 PC Board



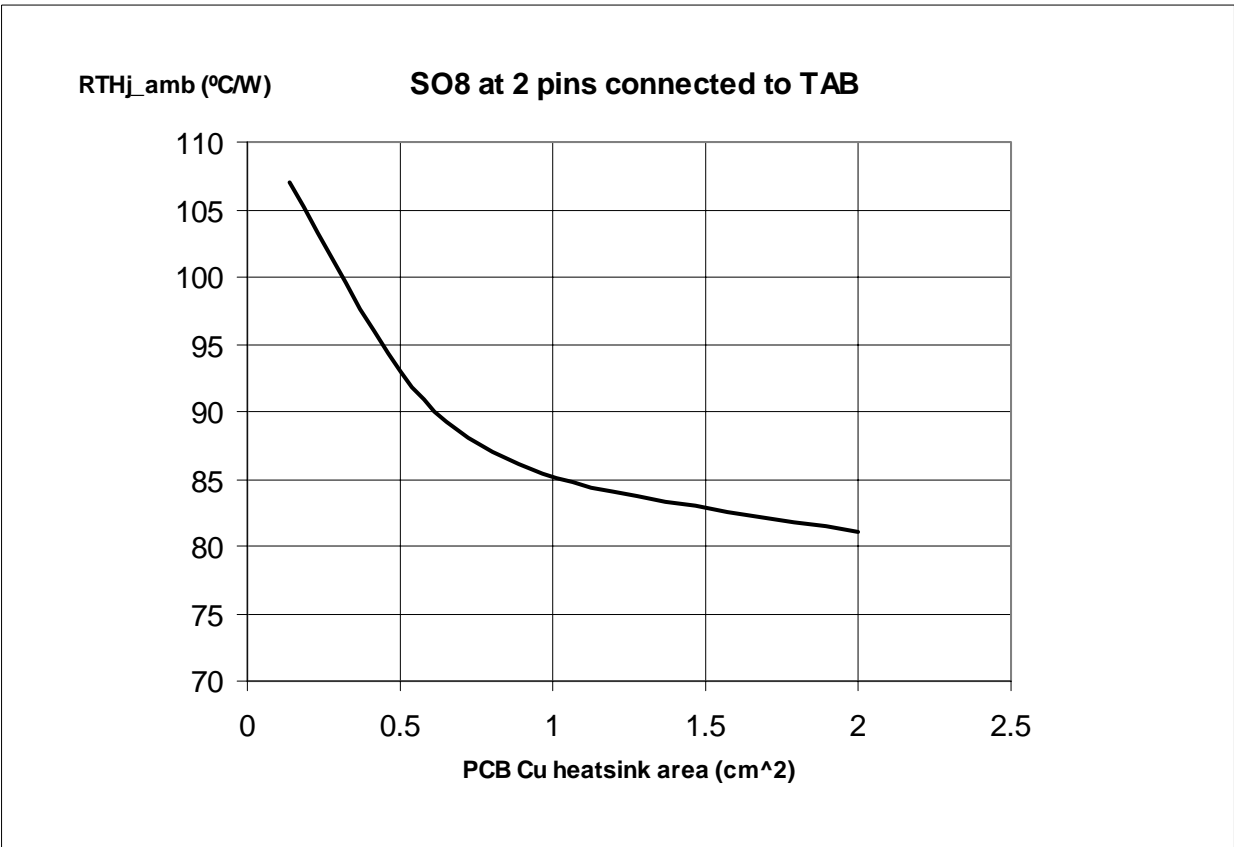
0.14cm²



2cm²

Layout condition of R_{th} and Z_{th} measurements (PCB FR4 area= 58mm x 58mm, PCB thickness=2mm, Cu thickness=35 μ m, Copper areas: 0.14cm², 2cm²).

$R_{thj-amb}$ Vs PCB copper area in open box free air condition

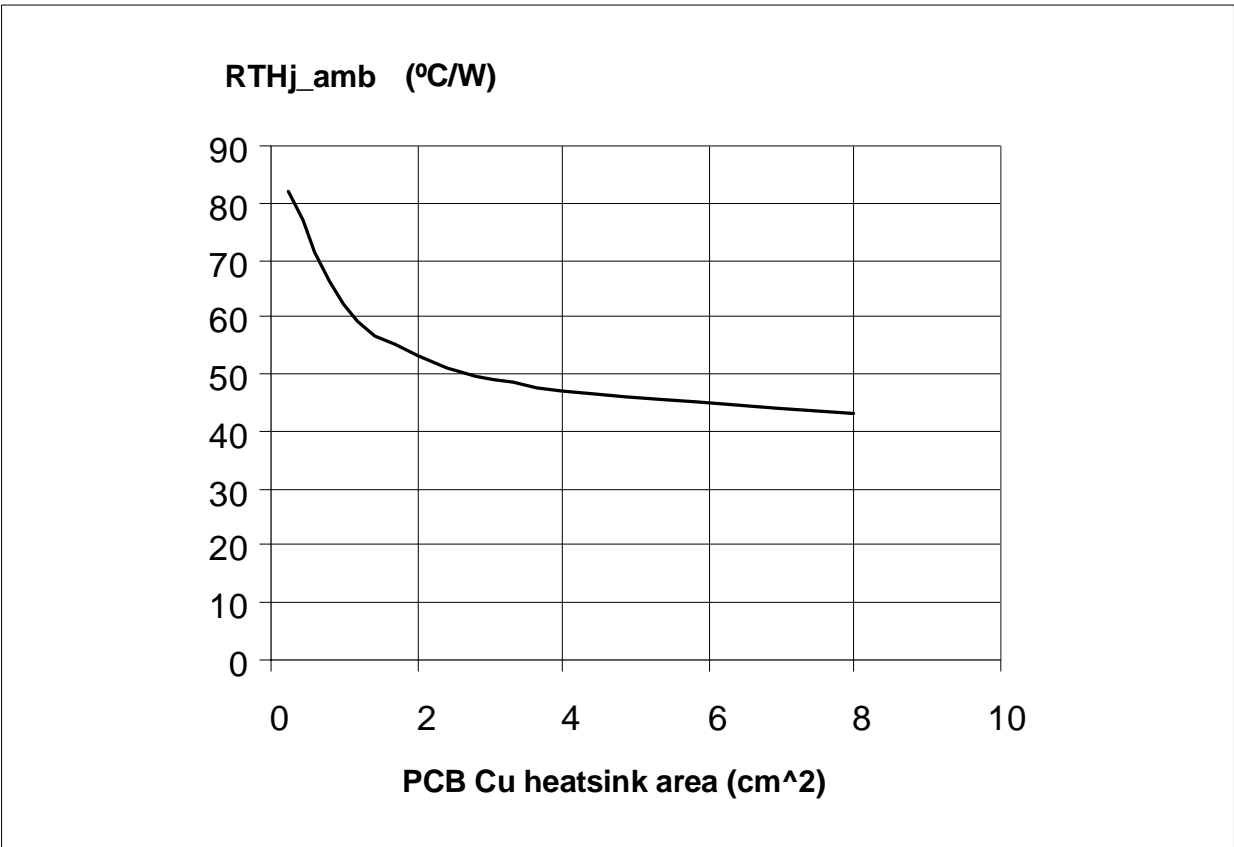


PPAK THERMAL DATA

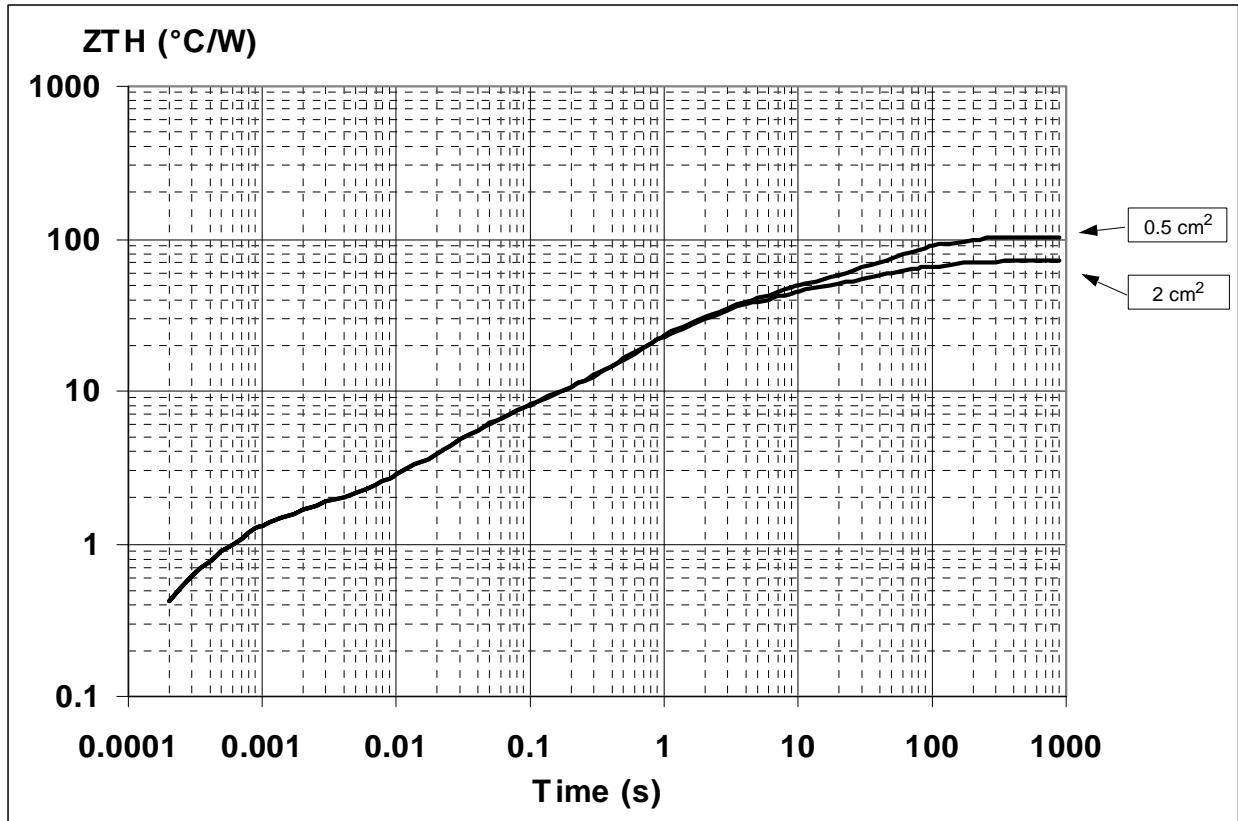
PPAK PC Board

Layout condition of R_{th} and Z_{th} measurements (PCB FR4 area= 60mm x 60mm, PCB thickness=2mm, Cu thickness=35 μ m, Copper areas: 0.44cm², 8cm²).

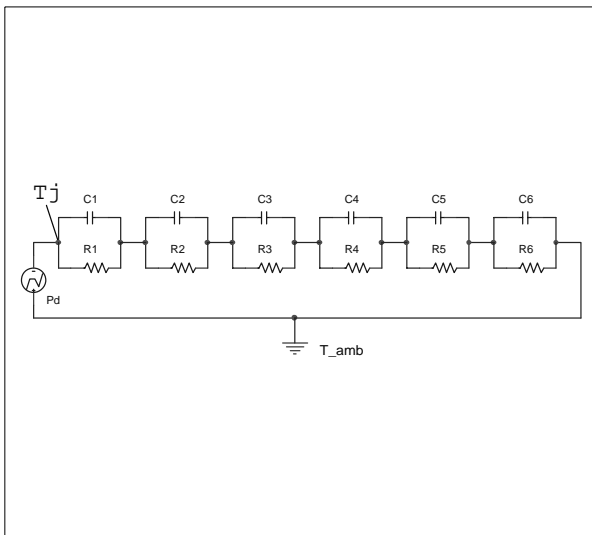
$R_{thj-amb}$ Vs PCB copper area in open box free air condition



SO-8 Thermal Impedance Junction Ambient Single Pulse



Thermal fitting model of a single channel HSD in SO-8



Pulse calculation formula

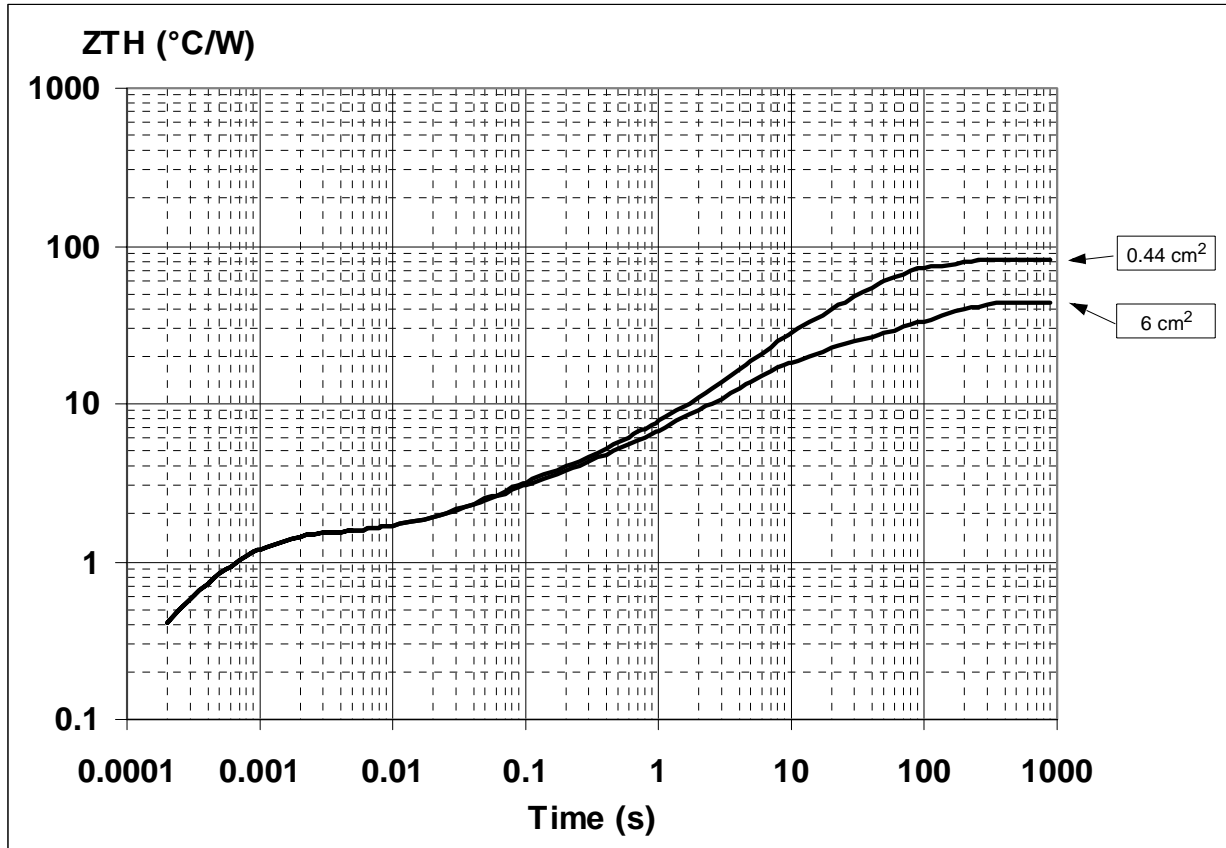
$$Z_{TH\delta} = R_{TH} \cdot \delta + Z_{THtp}(1 - \delta)$$

where $\delta = t_p/T$

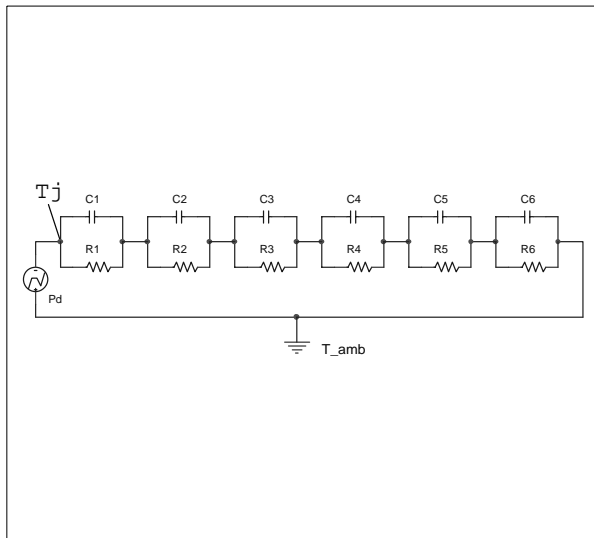
Thermal Parameter

	Area/island (cm ²)	
	0.14	2
R1 (°C/W)	0.24	
R2 (°C/W)	1.2	
R3 (°C/W)	4.5	
R4 (°C/W)	21	
R5 (°C/W)	16	
R6 (°C/W)	58	28
C1 (W.s/°C)	0.00015	
C2 (W.s/°C)	0.0005	
C3 (W.s/°C)	7.50E-03	
C4 (W.s/°C)	0.045	
C5 (W.s/°C)	0.35	
C6 (W.s/°C)	1.05	2

PPAK Thermal Impedance Junction Ambient Single Pulse



Thermal fitting model of a single channel HSD in PPAK



Pulse calculation formula

$$Z_{TH\delta} = R_{TH} \cdot \delta + Z_{THtp}(1 - \delta)$$

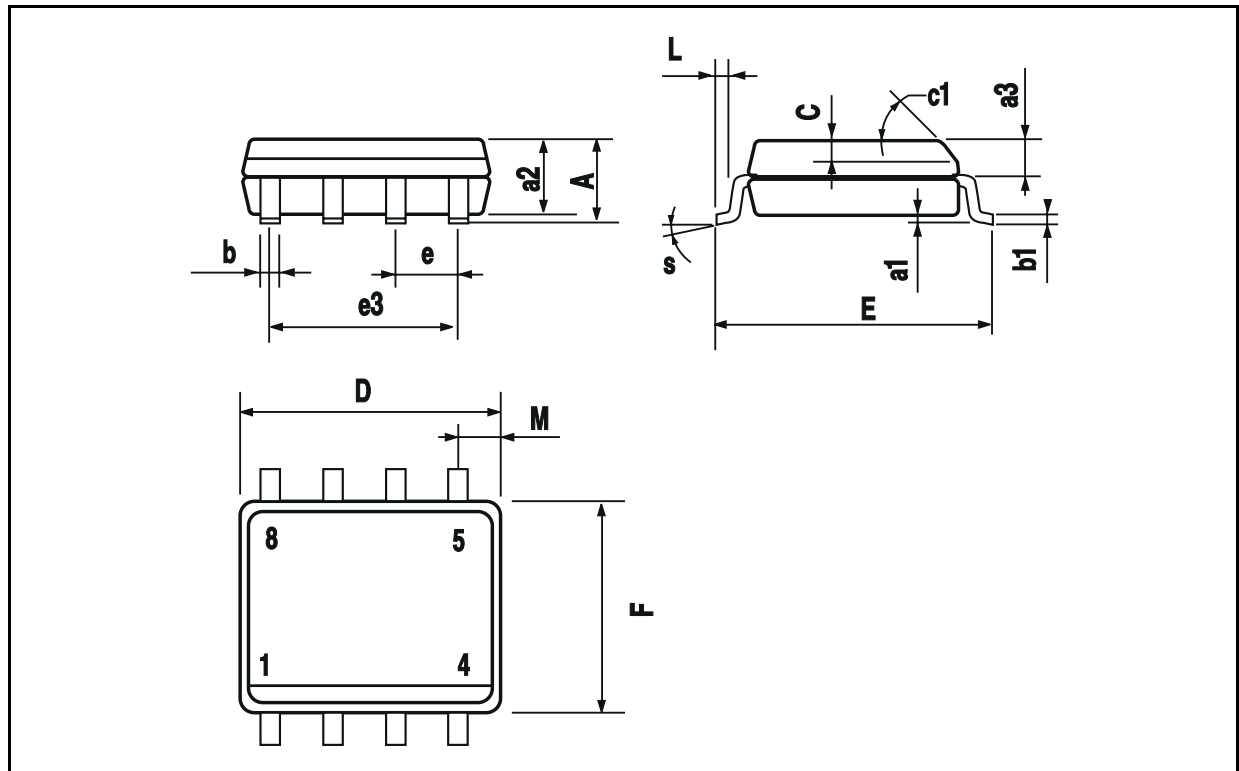
where $\delta = t_p / T$

Thermal Parameter

Area/island (cm ²)	0.44	6
R1 (°C/W)	0.04	
R2 (°C/W)	0.25	
R3 (°C/W)	0.3	
R4 (°C/W)	2	
R5 (°C/W)	15	
R6 (°C/W)	61	24
C1 (W.s/°C)	0.0008	
C2 (W.s/°C)	0.007	
C3 (W.s/°C)	0.02	
C4 (W.s/°C)	0.3	
C5 (W.s/°C)	0.45	
C6 (W.s/°C)	0.8	5

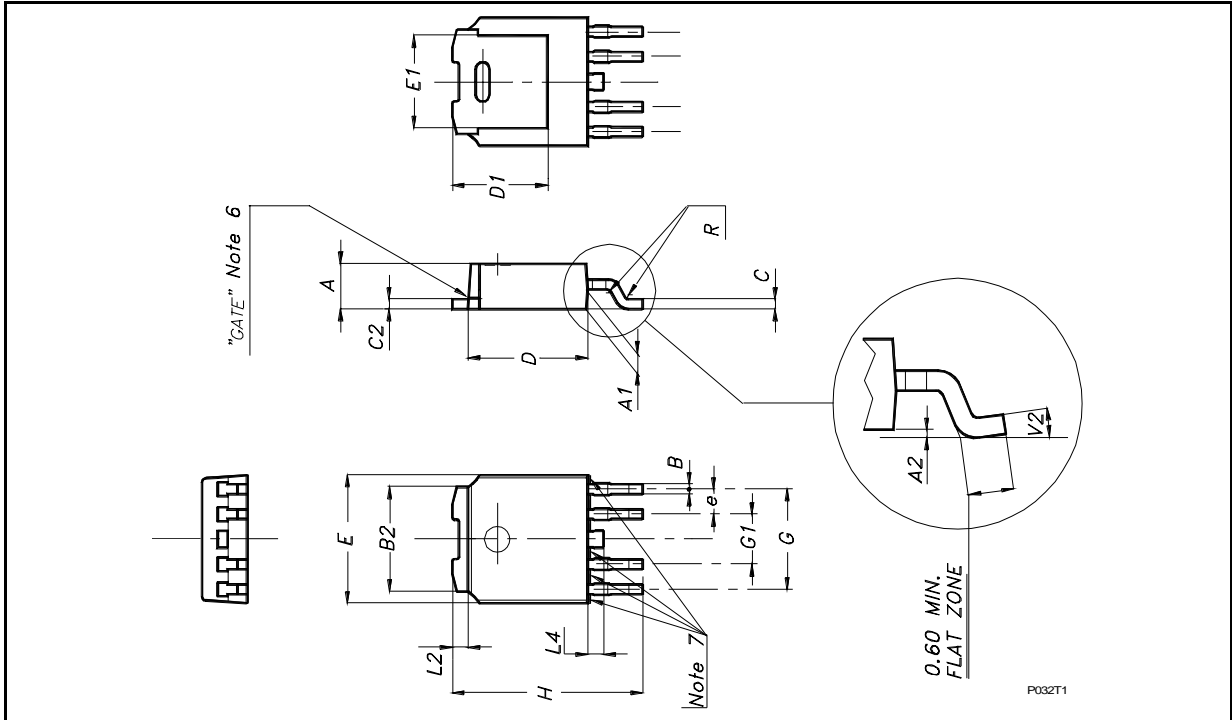
SO-8 MECHANICAL DATA

DIM.	mm.			inch		
	MIN.	TYP.	MAX.	MIN.	TYP.	MAX.
A			1.75			0.068
a1	0.1		0.25	0.003		0.009
a2			1.65			0.064
a3	0.65		0.85	0.025		0.033
b	0.35		0.48	0.013		0.018
b1	0.19		0.25	0.007		0.010
C	0.25		0.5	0.010		0.019
c1	45 (typ.)					
D	4.8		5	0.188		0.196
E	5.8		6.2	0.228		0.244
e		1.27			0.050	
e3		3.81			0.150	
F	3.8		4	0.14		0.157
L	0.4		1.27	0.015		0.050
M			0.6			0.023
S	8 (max.)					
L1	0.8		1.2	0.031		0.047

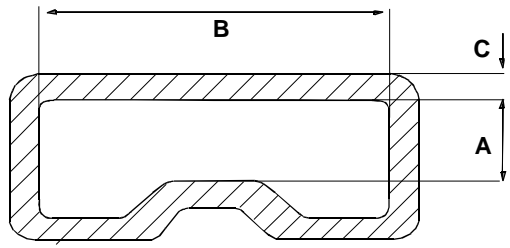


PPAK MECHANICAL DATA

DIM.	MIN.	TYP	MAX.
A	2.20		2.40
A1	0.90		1.10
A2	0.03		0.23
B	0.40		0.60
B2	5.20		5.40
C	0.45		0.60
C2	0.48		0.60
D1		5.1	
D	6.00		6.20
E	6.40		6.60
E1		4.7	
e		1.27	
G	4.90		5.25
G1	2.38		2.70
H	9.35		10.10
L2		0.8	1.00
L4	0.60		1.00
R		0.2	
V2	0°		8°
Package Weight	Gr. 0.3		



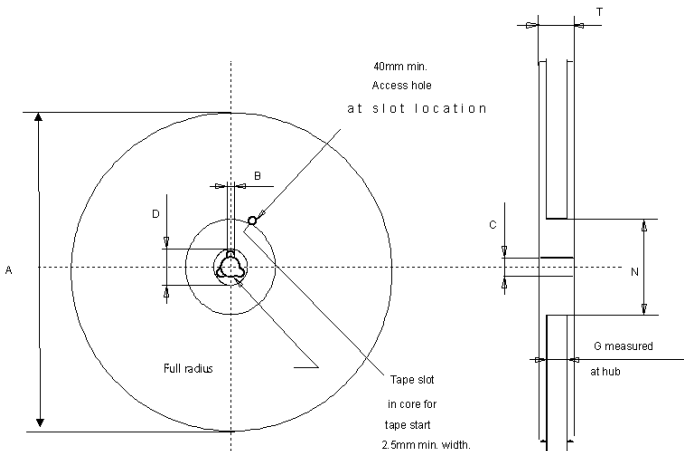
SO-8 TUBE SHIPMENT (no suffix)



Base Q.ty	100
Bulk Q.ty	2000
Tube length (± 0.5)	532
A	3.2
B	6
C (± 0.1)	0.6

All dimensions are in mm.

TAPE AND REEL SHIPMENT (suffix "13TR")



Base Q.ty	2500
Bulk Q.ty	2500
A (max)	330
B (min)	1.5
C (± 0.2)	13
F	20.2
G (+ 2 / -0)	12.4
N (min)	60
T (max)	18.4

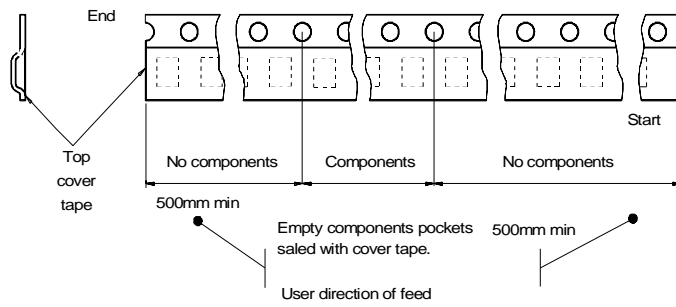
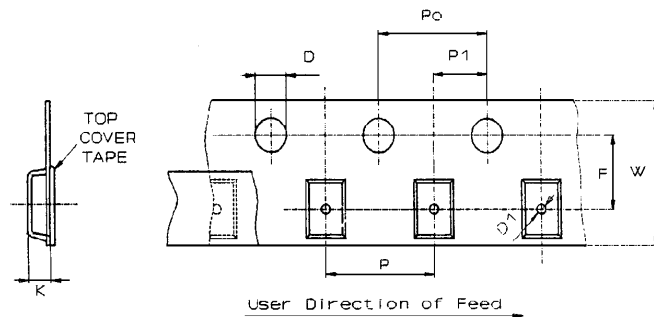
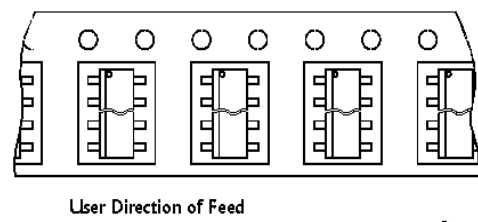
All dimensions are in mm.

TAPE DIMENSIONS

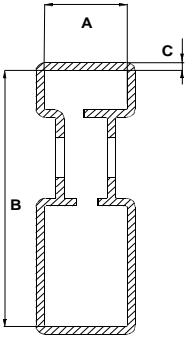
According to Electronic Industries Association (EIA) Standard 481 rev. A, Feb 1986

Tape width	W	12
Tape Hole Spacing	P0 (± 0.1)	4
Component Spacing	P	8
Hole Diameter	D (± 0.1/-0)	1.5
Hole Diameter	D1 (min)	1.5
Hole Position	F (± 0.05)	5.5
Compartment Depth	K (max)	4.5
Hole Spacing	P1 (± 0.1)	2

All dimensions are in mm.



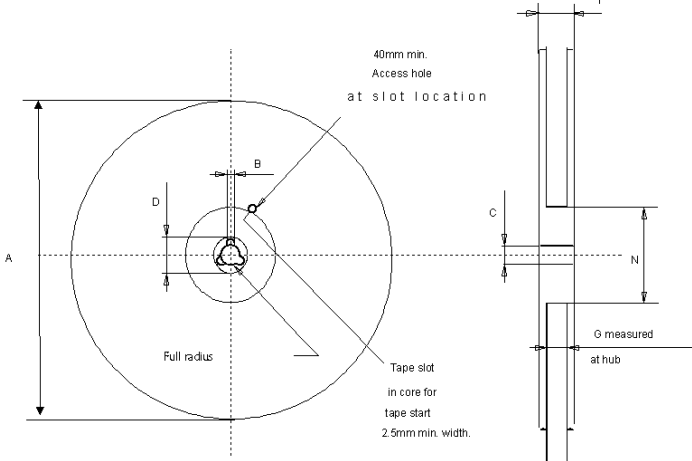
PPAK TUBE SHIPMENT (no suffix)



Base Q.ty	75
Bulk Q.ty	3000
Tube length (± 0.5)	532
A	6
B	21.3
C (± 0.1)	0.6

All dimensions are in mm.

TAPE AND REEL SHIPMENT (suffix "13TR")



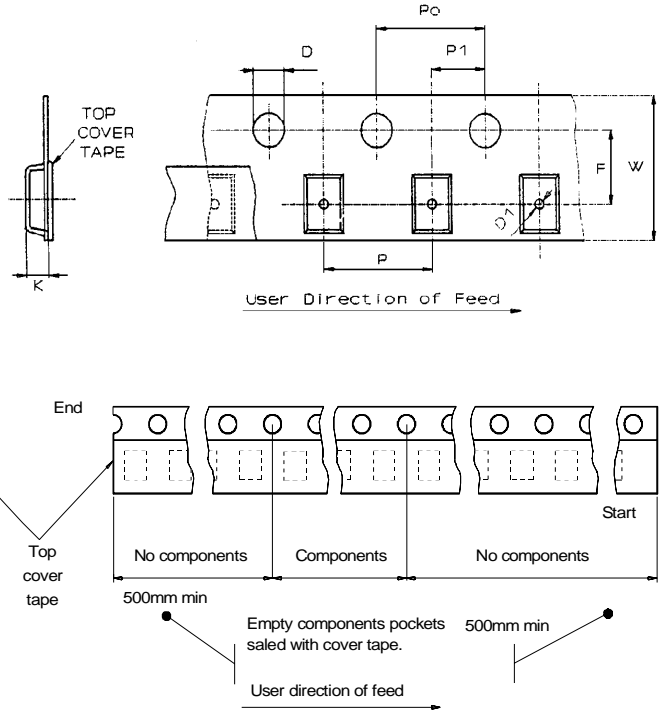
Base Q.ty	2500
Bulk Q.ty	2500
A (max)	330
B (min)	1.5
C (± 0.2)	13
F	20.2
G (+ 2 / -0)	16.4
N (min)	60
T (max)	22.4

All dimensions are in mm.

TAPE DIMENSIONS

According to Electronic Industries Association (EIA) Standard 481 rev. A, Feb 1986

Tape width	W	16
Tape Hole Spacing	P0 (± 0.1)	4
Component Spacing	P	8
Hole Diameter	D ($\pm 0.1/-0$)	1.5
Hole Diameter	D1 (min)	1.5
Hole Position	F (± 0.05)	7.5
Compartment Depth	K (max)	6.5
Hole Spacing	P1 (± 0.1)	2



All dimensions are in mm.

REVISION HISTORY

Date	Revision	Description of Changes
Jul. 2004	1	<ul style="list-style-type: none">- Current and voltage convention update (page 2).- "Configuration diagram (top view) & suggested connections for unused and n.c. pins" insertion (page 2).- 6cm² Cu condition insertion in Thermal Data table (page 3).- V_{CC} - OUTPUT DIODE section update (page 4).- PROTECTIONS note insertion (page 4).- Revision History table insertion (page 21).- Disclaimers update (page 22).

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